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Title: ELECTRONIC ASSEMBLY COMPRISING SOLDERABLE THERMAL INTERFACE AND METHODS OF MANUFACTURE

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UNITED STATES PATENT APPLICATION

ELECTRONIC ASSEMBLY COMPRISING SOLDERABLE THERMAL INTERFACE AND METHODS OF MANUFACTURE

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Electronic Assembly Comprising Solderable Thermal Interface and Methods of Manufacture

Technical Field of the Invention

The present invention relates generally to electronics packaging. More particularly, the present invention relates to an electronic assembly that includes an integrated circuit package comprising a solderable thermal interface between the integrated circuit and a heat spreader to dissipate heat generated in a high speed integrated circuit, and to manufacturing methods related thereto.

Background of the Invention

Integrated circuits (ICs) are typically assembled into packages by physically and electrically coupling them to a substrate made of organic or ceramic material. One or more IC packages can be physically and electrically coupled to a printed circuit board (PCB) to form an "electronic assembly". The "electronic assembly" can be part of an "electronic system". An "electronic system" is broadly defined herein as any product comprising an "electronic assembly". Examples of electronic systems include computers (e.g., desktop, laptop, hand-held, server, etc.), wireless communications devices (e.g., cellular phones, cordless phones, pagers, etc.), computer-related peripherals (e.g., printers, scanners, monitors, etc.), entertainment devices (e.g., televisions, radios, stereos, tape and compact disc players, video cassette recorders, MP3 (Motion Picture Experts Group, Audio Layer 3) players, etc.), and the like.

In the field of electronic systems there is an incessant competitive pressure among manufacturers to drive the performance of their equipment up while driving down production costs. This is particularly true regarding the packaging of ICs on substrates, where each new generation of packaging must provide increased

performance while generally being smaller or more compact in size. As the power demands of high performance IC processors approach and even exceed 100 watts per chip, with localized power densities exceeding 200 watts/square centimeter, the heat dissipating capability of the IC package must correspondingly increase.

An IC substrate may comprise a number of metal layers selectively patterned to provide metal interconnect lines (referred to herein as "traces"), and one or more electronic components mounted on one or more surfaces of the substrate. The electronic component or components are functionally connected to other elements of an electronic system through a hierarchy of electrically conductive paths that include the substrate traces. The substrate traces typically carry signals that are transmitted between the electronic components, such as ICs, of the system. Some ICs have a relatively large number of input/output (I/O) terminals, as well as a large number of power and ground terminals.

One of the conventional methods for mounting an IC on a substrate is called "controlled collapse chip connect" (C4). In fabricating a C4 package, the electrically conductive terminations or lands (generally referred to as "electrical contacts") of an IC component are soldered directly to corresponding lands on the surface of the substrate using reflowable solder bumps or balls. The C4 process is widely used because of its robustness and simplicity.

As the internal circuitry of ICs, such as processors, operates at higher and higher clock frequencies, and as ICs operate at higher and higher power levels, the amount of heat generated by such IC's can increase to unacceptable levels.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a significant need in the art for a method and apparatus for packaging an IC on a substrate that minimizes heat dissipation problems associated with high clock frequencies and high power densities.

Brief Description of the Drawings

FIG. 1 is a block diagram of an electronic system incorporating at least one

electronic assembly with a solderable thermal interface in accordance with one embodiment of the invention;

FIG. 2 illustrates a cross-sectional representation of an integrated circuit package, in accordance with one embodiment of the invention;

FIG. 3 illustrates a cross-sectional representation of a solderable thermal interface between a die and a lid or integrated heat spreader, in accordance with one embodiment of the invention; and

FIG. 4 is a flow diagram of a method of packaging a die, in accordance with one embodiment of the invention.

Detailed Description of Embodiments of the Invention

In the following detailed description of embodiments of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical, and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

The present invention provides a solution to thermal dissipation problems that are associated with prior art packaging of integrated circuits that operate at high clock speeds and high power levels by employing a highly conductive solder material as a thermal interface between an IC die and a heat spreader. Various embodiments are illustrated and described herein.

In one embodiment, an IC die is mounted to an organic land grid array (OLGA) substrate using C4 technology. An integrated heat spreader is attached to the back surface of the die using a highly conductive solderable thermal interface material after suitable preparation of the die and heat spreader surfaces. A

solderable thermal interface material is selected that has a relatively low melting point, in order to minimize thermal stresses in the package that can be generated, because the silicon die has a relatively low thermal coefficient of expansion (TCE) compared to the TCE of the OLGA substrate. By reducing thermal stresses, the package is less likely to experience warpage when it is subjected to heat, for example during solder reflow.

The solderable thermal interface material also has excellent thermal conductive properties. The integrated heat spreader can also be coupled to the OLGA substrate around the die periphery with a suitable sealant in order to provide mechanical strength.

In addition to the foregoing advantages, the use of a low melting point solder as a thermal interface material avoids many problems associated with the use of polymeric thermal interface materials (e.g. those containing silver or aluminum), such as resin separation, out-gassing, delamination, pump-out, and so forth.

FIG. 1 is a block diagram of an electronic system 1 incorporating at least one electronic assembly 4 with a solderable thermal interface in accordance with one embodiment of the invention. Electronic system 1 is merely one example of an electronic system in which the present invention can be used. In this example, electronic system 1 comprises a data processing system that includes a system bus 2 to couple the various components of the system. System bus 2 provides communications links among the various components of the electronic system 1 and can be implemented as a single bus, as a combination of busses, or in any other suitable manner.

Electronic assembly 4 is coupled to system bus 2. Electronic assembly 4 can include any circuit or combination of circuits. In one embodiment, electronic assembly 4 includes a processor 6 which can be of any type. As used herein, "processor" means any type of computational circuit, such as but not limited to a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, a graphics processor, a digital signal processor (DSP), or any other type of processor or processing circuit.

Other types of circuits that can be included in electronic assembly 4 are a custom circuit, an application-specific integrated circuit (ASIC), or the like, such as, for example, one or more circuits (such as a communications circuit 7) for use in wireless devices like cellular telephones, pagers, portable computers, two-way radios, and similar electronic systems. The IC can perform any other type of function.

Electronic system 1 can also include an external memory 10, which in turn can include one or more memory elements suitable to the particular application, such as a main memory 12 in the form of random access memory (RAM), one or more hard drives 14, and/or one or more drives that handle removable media 16 such as floppy diskettes, compact disks (CDs), digital video disk (DVD), and the like.

Electronic system 1 can also include a display device 8, a speaker 9, and a keyboard and/or controller 20, which can include a mouse, trackball, game controller, voice-recognition device, or any other device that permits a system user to input information into and receive information from the electronic system 1.

FIG. 2 illustrates a cross-sectional representation of an integrated circuit (IC) package, in accordance with one embodiment of the invention. The IC package comprises a die 50 mounted on an organic land grid array (OLGA) substrate 54, and a lid or integrated head spreader (IHS) 52. While an OLGA substrate is shown, the present invention is not limited to use with an OLGA substrate, and any other type of substrate can be employed.

The IC package illustrated in FIG. 2 can form part of electronic assembly 4 shown in FIG. 1. Die 50 can be of any type. In one embodiment, die 50 is a processor.

In FIG. 2, die 50 comprises a plurality of signal conductors (not shown) that terminate in pads on the bottom surface of die 50 (not shown). These pads can be coupled to corresponding lands 68 representing signal, power, or ground nodes on OLGA substrate 54 by appropriate connections such as C4 solder bumps 66. A suitable underfill 62, such as an epoxy material, can be used to surround C4 solder bumps 66 to provide mechanical stability and strength.

Still referring to FIG. 2, lid or IHS 52 forms a cover over die 50. IHS 52 is thermally coupled to a surface of die 50 through a suitable solderable thermal interface 60. Die 50 can thus dissipate a substantial amount of heat through thermal interface 60 to IHS 52. The solderable thermal interface 60 comprises a material that is capable of conducting heat at a relatively high rate, and that has a relatively low melting point to minimize thermal stresses in the package when it is subjected to heat, for example during solder reflow.

IHS 52 can be mechanically supported by coupling its wall or support member 53 to the surface of OLGA substrate 54 through a suitable sealant 64. In one embodiment, the wall or support member 53 is located at the periphery of IHS 52. However, in other embodiments IHS 52 can extend beyond the support member 53. For example, a heat spreader of any shape can be formed as part of or attached to IHS 52, in order to increase the rate of heat dissipation from die 50.

OLGA substrate 54 can be of any type, including a multi-layer substrate. OLGA substrate 54 can be mounted to an additional substrate 70, such as a printed circuit board (PCB) or card. OLGA substrate 54 can comprise, for example, a plurality of lands 57 that can be mechanically and electrically coupled to corresponding lands 59 of substrate 70 by suitable connectors such as ball grid array (BGA) solder balls 58.

While a BGA arrangement 56 is illustrated in FIG. 2 for coupling OLGA substrate 54 to substrate 70, the present invention is not limited to use with a BGA arrangement, and it can be used with any other type of packaging technology, e.g. land grid array (LGA), chip scale package (CSP), or the like. Further, the present invention is not to be construed as limited to use in C4 packages, and it can be used with any other type of IC package where the herein-described features of the present invention provide an advantage.

The fabrication of an IC package comprising a solderable thermal interface 60 will now be described.

Fabrication

In order to successfully fabricate an IC package with the advantages described above, it is important to have a die surface that is readily solderable. It is also important to have an IHS that is readily solderable. In addition, it is important to use a suitable solder material. Further, it is important to utilize a suitable process for forming a reliable thermal interface between the die and the IHS. Each of the above-mentioned factors will now be described in sufficient detail to enable one of ordinary skill in the art to understand and practice the invention.

FIG. 3 illustrates a cross-sectional representation of a thermal interface (also referred to herein as a thermally conductive element) 60 between a die 50 and a lid or integrated heat spreader (IHS) 52, in accordance with one embodiment of the invention.

For good solderability of the thermal interface 60 to the die 50, according to one embodiment of the invention, one or more metal layers 82, 84, and 86 are deposited on the die surface that is to be coupled via thermal interface 60 to the IHS 52. Before deposition of the one or more metal layers 82, 84, and/or 86, the wafer surface can be prepared with a sputter etch, if desired, to improve the adhesion of the adhesion layer 82 to the die surface; however, a sputter etch is not essential. Nor is the condition of the wafer surface essential. The wafer surface can be in unpolished, polished, or back-ground form.

Next, an adhesion layer 82 of a metal that adheres well to silicon, silicon oxide, or silicon nitride, such as titanium (Ti), is deposited onto the etched surface. In one embodiment, a 500 Angstrom layer of titanium is sputtered onto the etched surface. Chromium (Cr), vanadium (V), and possibly zirconium (Zr) could be substituted for Ti.

Next, a second metal layer 84, such as nickel-vanadium (NiV), is deposited. In one embodiment, a 3500 Angstrom layer of NiV is sputtered onto the Ti layer. A purpose of layer 84 is to serve as a diffusion barrier to prevent any reaction of solder in the thermal interface 60 with the adhesion layer 82, which could result in possible delamination of the thermal interface 60 from the die 50. Layer 84 is not necessarily required, depending upon the composition of the adhesion layer 82, the solder

material in the thermal interface 60, and the thermal treatment during the reflow operation.

Next, a third metal layer 86, such as gold (Au), is deposited. In one embodiment, a 600 Angstrom layer of Au is sputtered onto the NiV layer. Any metal that "wets" the chosen solder material in the thermal interface 60 could be substituted for gold. Nickel is one example.

For good solderability of the thermal interface 60 to the lid or IHS 52, one or more metal or solderable organic layers 88 are deposited onto the appropriate surface of the IHS 52. In one embodiment, IHS 52 comprises copper (Cu); in another embodiment IHS 52 comprises aluminum-silicon-carbide (AlSiC). For an IHS 52 comprising either Cu or AlSiC, a 2-5 micron thick layer 88 of Ni is deposited on the lower surface of IHS 52. Electroless Ni plating is carried out in a Niklad 767 bath using a medium force solution. Any metal that "wets" the chosen solder material in the thermal interface 60 could be substituted for nickel. Gold is one example. A combination of metals or alloys could also be substituted for the single layer 88 shown in FIG. 3.

For a suitable solder material, any of the solder alloys, or a combination thereof, listed in Table 1 would be effective. All are commercially available from Indium Corporation of America, Utica, NY under the corresponding Indalloy® No. In one embodiment, the solder can be integrated with a no-clean flux vehicle to form a solder paste with an 89% loading of the selected solder alloy.

Composition	Liquidus (°C)	Solidus (°C)	Thermal Conductivity Watts/Meter °C	Indalloy No.
58% Bismuth (Bi) / 42% Tin (Sn)	138	138	19	281
97% Indium (In) / 3% Silver (Ag)	143	143	73	290
80% In / 15% Lead (Pb) / 5% Ag	154	149	43	2
100% In	157	157	86	4

Table 1

A suitable process for forming a reliable solderable thermal interface between the die and the IHS will now be described. Solder paste is first applied to the back side of the die. Alternatively, the solder paste could be applied to the surface of IHS 52 that faces the back side of the die. Then a suitable sealant (64, FIG. 2) is applied to the OLGA substrate 54 where the periphery or boundary of IHS 52 will make contact when it is positioned over the die 50. Next, the IHS 52 is placed, and an appropriate force can be applied, for example using a spring, to hold IHS 52 in position. The package is then put into a suitable heating environment, such as a flow furnace, for solder reflow. In one embodiment of the method, during solder reflow, the maximum zone temperature in the furnace is maintained at liquidus of the solder material + 30°C, and the time above liquidus is approximately 60 seconds. Following solder join of the thermal interface, the sealant at the IHS boundary is cured in a conventional oven.

The above-described choice of materials, geometry, number of layers, etching, deposition, and assembly can all be varied by one of ordinary skill in the art to optimize the thermal performance of the package. However, an unoptimized embodiment of the present invention has been demonstrated to provide a substantial

thermal margin for IC's operating at high clock frequencies and high power levels, and without any adverse impact on package reliability.

Any suitable method, or combination of different methods, for depositing the metal layers can be used, such as sputtering, vapor, electrical, screening, stenciling, chemical including chemical vapor deposition (CVD), vacuum, and so forth.

The particular implementation of the IC package is very flexible in terms of the orientation, size, number, and composition of its constituent elements. Various embodiments of the invention can be implemented using various combinations of substrate technology, IHS technology, thermal interface material, and sealant to achieve the advantages of the present invention. The structure, including types of materials used, dimensions, layout, geometry, and so forth, of the IC package can be built in a wide variety of embodiments, depending upon the requirements of the electronic assembly of which it forms a part.

FIGS. 2 and 3 are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated, while others may be minimized. FIGS. 2 and 3 are intended to illustrate various implementations of the invention that can be understood and appropriately carried out by those of ordinary skill in the art.

FIG. 4 is a flow diagram of a method of packaging a die, in accordance with one embodiment of the invention. The method begins at 100.

In 101, at least one metal layer is formed on a surface of a die. In one embodiment, as described above, individual layers of titanium, nickel-vanadium, and gold are successively deposited on the upper surface of die 50 (FIG. 3). One or more alloys of these metals could also be used.

In 103, at least one metal layer is formed on a surface of the lid. In one embodiment, as described above, a layer of nickel is deposited on the lower surface of lid or IHS 52 (FIG. 3).

In 105, the die is mounted on a substrate. In one embodiment, as described above, the substrate is an organic substrate, and the die is C4 mounted using a land grid array (LGA) arrangement. It is to be noted that substrates comprising one or more organic materials, such as epoxies, acrylates, polyimides, polyurethanes,

polysulfides, resin-glass weave (e.g. FR-4), nylons, and other similar materials, have a relatively high thermal coefficient of expansion compared with that of the die.

In 107, solder material having a relatively high thermal conductivity and a relatively low melting point is applied to the at least one metal layer of the die. In securing the IHS to the die, it is desirable to employ a solder material having a relatively low melting point to minimize warpage problems when the package is subjected to heat. In one embodiment, as described above, the solder material is any of those listed in Table 1; however, other solder materials besides those listed in Table 1 could be used, provided that they have the qualities previously mentioned. Alternatively, the solder material could be applied to the at least one metal layer on the surface of the lid. The solder material can be applied at any suitable stage in the fabrication process.

In 109, a suitable sealant is applied to the surface of the substrate where the support member 53 (FIG. 2) of IHS 52 will contact it.

In 111, the IHS is placed and aligned so that the inner surface of the IHS contacts the layer of solder material and, concurrently, the support member 53 of IHS 52 contacts the sealant. A spring (not shown) is also placed to secure the assembly with respect to an assembly carrier (not shown).

In 113, the solder material is melted or reflowed by heating so that, when it has cooled, the IHS 52 is physically and thermally coupled to the upper surface of the top metal layer 86 (FIG. 3) on die 50.

In 115, the sealant is cured, for example, by heating, to provide mechanical coupling of the assembly. Post cure, the securing spring is removed from the assembly carrier. The method ends in 120.

The operations described above with respect to the methods illustrated in FIG. 4 can be performed in a different order from those described herein. For example, it will be understood by those of ordinary skill that 103 could be carried out prior to 101, that 107 could be carried out prior to 105, and 109 could be carried out prior to 107.

Conclusion

The present invention provides for an electronic assembly and methods of manufacture thereof that minimize thermal dissipation problems associated with high power delivery. An electronic system and/or data processing system that incorporates one or more electronic assemblies that utilize the present invention can handle the relatively high power densities associated with high performance integrated circuits, and such systems are therefore more commercially attractive.

As shown herein, the present invention can be implemented in a number of different embodiments, including an assembly for a die, an integrated circuit package, an electronic assembly, an electronic system, a data processing system, and a method for packaging an integrated circuit. Other embodiments will be readily apparent to those of ordinary skill in the art. The elements, materials, geometries, dimensions, and sequence of operations can all be varied to suit particular packaging requirements.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

CLAIMS

What is claimed is:

1. An assembly for a die comprising:
a lid; and
a solderable thermally conductive element to couple a die to the lid.

2. The assembly recited in claim 1 wherein the lid comprises material from the group consisting of copper and aluminum-silicon-carbide.

3. The assembly recited in claim 1 wherein the solderable thermally conductive element comprises material, including one or more alloys, from the group consisting of tin, bismuth, silver, indium, and lead.

4. The assembly recited in claim 1 wherein the lid comprises at least one metal or organic layer to which the thermally conductive element can be coupled.

5. The assembly recited in claim 4 wherein the at least one metal or organic layer comprises nickel or gold.

6. The assembly recited in claim 1 and further comprising:
a die comprising at least one metal layer to which the solderable thermally conductive element can be coupled.

7. The assembly recited in claim 6 wherein the at least one metal layer comprises material, including one or more alloys, from the group consisting of titanium, chromium, zirconium, nickel, vanadium, and gold.

8. An integrated circuit package comprising:
a substrate;
a die positioned on a surface of the substrate;
a lid positioned over the die; and
a solderable thermally conductive element coupling the die and the lid.

9. The integrated circuit package recited in claim 8 wherein the lid comprises a support member coupled to the substrate.

10. The integrated circuit package recited in claim 8 wherein the lid comprises material from the group consisting of copper and aluminum-silicon-carbide.

11. The integrated circuit package recited in claim 8 wherein the lid comprises at least one metal or organic layer to which the thermally conductive element is coupled.

12. The integrated circuit package recited in claim 11 wherein the at least one metal or organic layer comprises nickel or gold.

13. The integrated circuit package recited in claim 8 wherein the solderable thermally conductive element comprises material, including one or more alloys, from the group consisting of tin, bismuth, silver, indium, and lead.

14. The integrated circuit package recited in claim 8 wherein the substrate is an organic substrate and wherein the die is coupled to the substrate through a land grid array.

15. The integrated circuit package recited in claim 8 wherein the die comprises at least one metal layer to which the thermally conductive element is coupled.

16. The integrated circuit package recited in claim 15 wherein the at least one metal layer comprises material, including one or more alloys, from the group consisting of titanium, chromium, zirconium, nickel, vanadium, and gold.

17. An electronic assembly comprising:

at least one integrated circuit package comprising:

a substrate;

a die positioned on a surface of the substrate;

a lid positioned over the die; and

a solderable thermally conductive element coupling the die and the lid.

18. The electronic assembly recited in claim 17 wherein the lid comprises a support member coupled to the substrate.

19. The electronic assembly recited in claim 17 wherein the solderable thermally conductive element comprises material, including one or more alloys, from the group consisting of tin, bismuth, silver, indium, and lead.

20. The electronic assembly recited in claim 17 wherein the substrate is an organic substrate and wherein the die is coupled to the substrate through a land grid array.

21. An electronic system comprising an electronic assembly having at least one integrated circuit package comprising:

a substrate;

a die positioned on a surface of the substrate;

a lid positioned over the die; and

a solderable thermally conductive element coupling the die and the lid.

22. The electronic system recited in claim 21 wherein the solderable thermally conductive element comprises material, including one or more alloys, from the group consisting of tin, bismuth, silver, indium, and lead.

23. The electronic system recited in claim 21 wherein the substrate is an organic substrate, wherein the die is coupled to the substrate through a land grid array, and wherein the lid comprises a support member coupled to the substrate.

24. A data processing system comprising:

a bus coupling components in the data processing system;

a display coupled to the bus;

external memory coupled to the bus; and

a processor coupled to the bus and comprising an electronic assembly including at least one integrated circuit package comprising:

a substrate;

a die positioned on a surface of the substrate;

a lid positioned over the die; and

a solderable thermally conductive element coupling the die and the lid.

25. The data processing system recited in claim 24 wherein the solderable thermally conductive element comprises material, including one or more alloys, from the group consisting of tin, bismuth, silver, indium, and lead.

26. The data processing system recited in claim 24 wherein the substrate is an organic substrate and wherein the die is coupled to the substrate through a land grid array.

27. A method of fabricating an integrated circuit package, the method comprising:

forming at least one metal layer on a surface of a die;

mounting the die on a substrate;

positioning a surface of a lid adjacent the layer of solder material; and

applying solder material between the at least one metal layer and the surface of the lid;

melting the solder material to physically couple the lid to the die.

28. The method recited in claim 27 wherein the solder material has a relatively high thermal conductivity and a relatively low melting point.

29. The method recited in claim 27 wherein the substrate comprises organic material having a relatively high thermal coefficient of expansion relative to that of the die.

30. The method recited in claim 27 and further comprising forming at least one metal or organic layer on the surface of the lid prior to applying solder material.

Electronic Assembly Comprising Solderable Thermal Interface and Methods of Manufacture

5

Abstract of the Disclosure

To accommodate high power densities associated with high performance integrated circuits, heat is dissipated from a surface of a die through a solderable 10 thermal interface to a lid or integrated heat spreader. In one embodiment, the die is mounted on an organic substrate using a C4 and land grid array arrangement. In order to maximize thermal dissipation from the die while minimizing warpage of the package when subjected to heat, due to the difference in thermal coefficients of expansion between the die and the organic substrate, a thermal interface is used that 15 has a relatively low melting point in addition to a relatively high thermal conductivity. Methods of fabrication, as well as application of the package to an electronic assembly, an electronic system, and a data processing system, are also described.

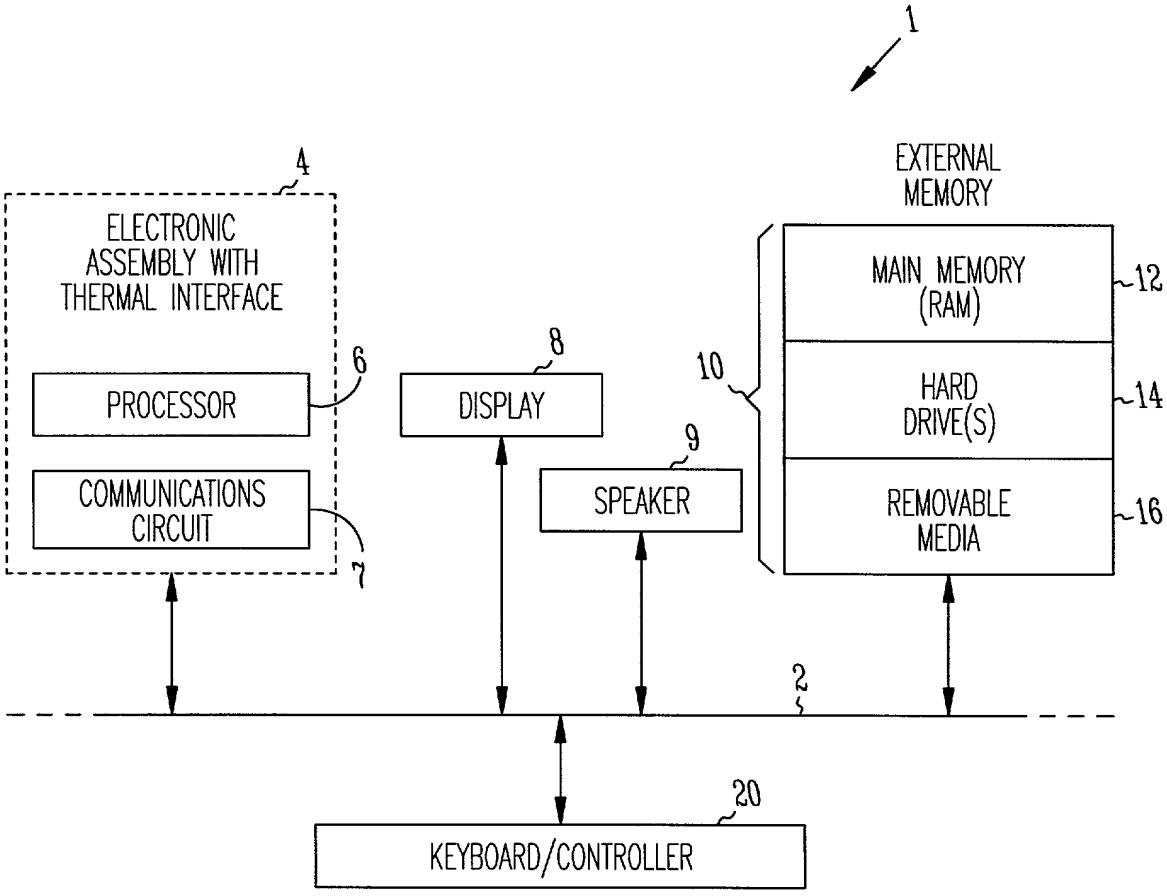
1
4
ELECTRONIC ASSEMBLY WITH THERMAL INTERFACE
PROCESSOR
6
COMMUNICATIONS CIRCUIT
7
8
DISPLAY
9
SPEAKER
10
EXTERNAL MEMORY
MAIN MEMORY (RAM)
12
HARD DRIVE(S)
14
REMOVABLE MEDIA
16
2
20
KEYBOARD/CONTROLLER

Fig. 1

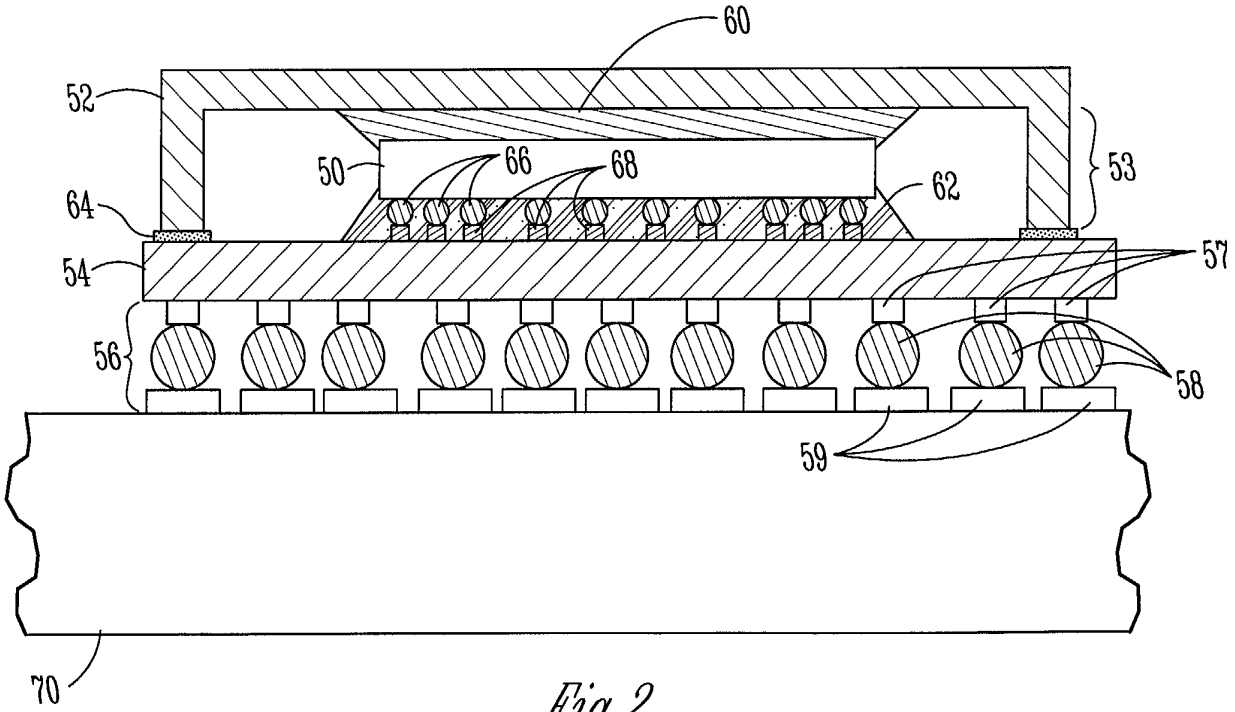

Fig.2

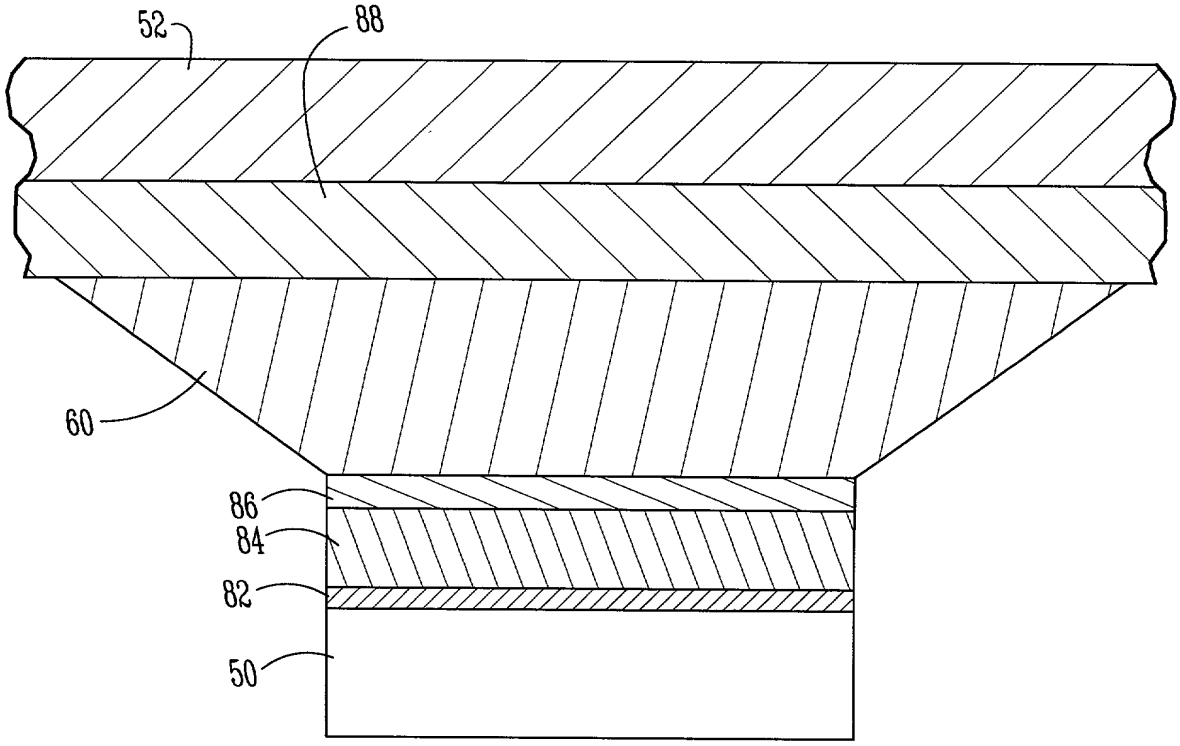

Fig. 3

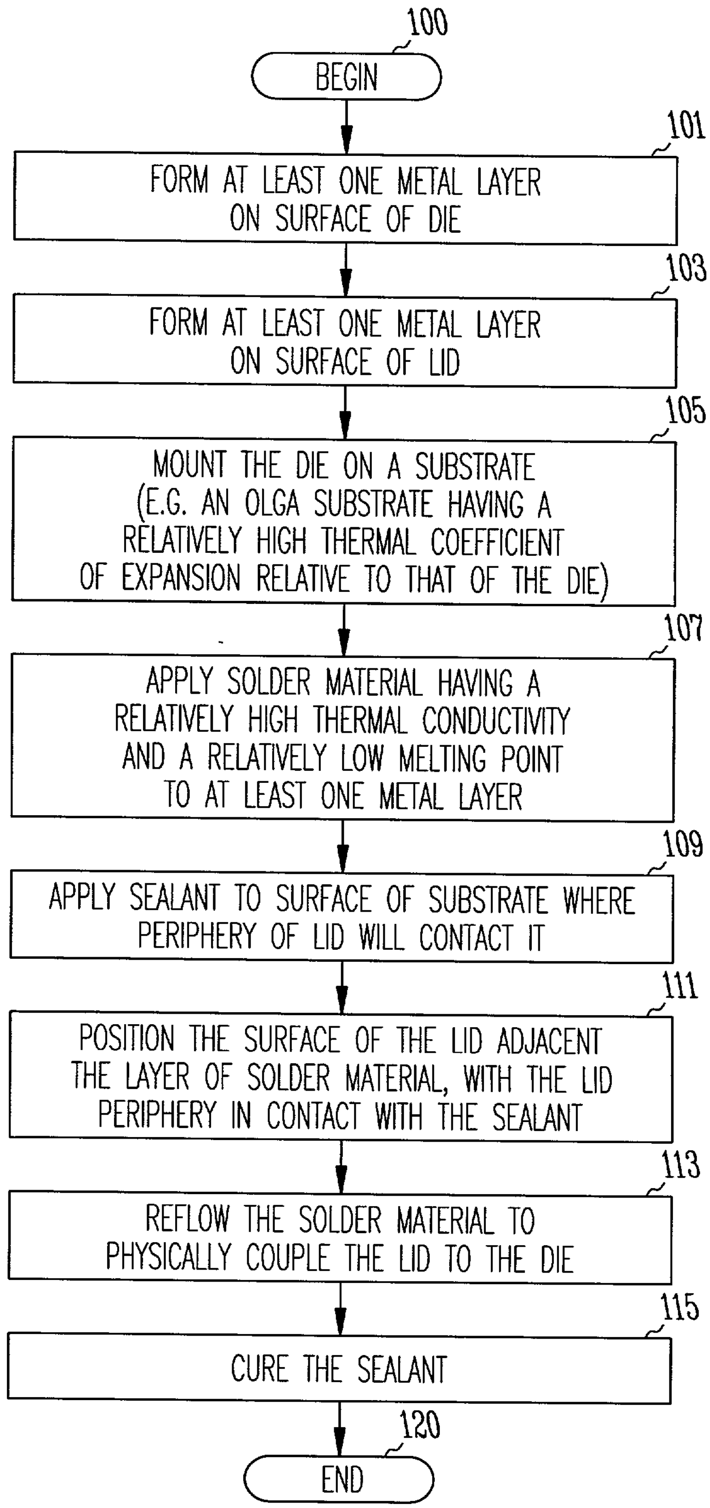
100
BEGIN
101
FORM AT LEAST ONE METAL LAYER ON SURFACE OF DIE
103
FORM AT LEAST ONE METAL LAYER ON SURFACE OF LID
105
MOUNT THE DIE ON A SUBSTRATE (E.G. AN OLGA SUBSTRATE HAVING A RELATIVELY HIGH THERMAL COEFFICIENT OF EXPANSION RELATIVE TO THAT OF THE DIE)
107
APPLY SOLDER MATERIAL HAVING A RELATIVELY HIGH THERMAL CONDUCTIVITY AND A RELATIVELY LOW MELTING POINT TO AT LEAST ONE METAL LAYER
109
APPLY SEALANT TO SURFACE OF SUBSTRATE WHERE PERIPHERY OF LID WILL CONTACT IT
111
POSITION THE SURFACE OF THE LID ADJACENT THE LAYER OF SOLDER MATERIAL, WITH THE LID PERIPHERY IN CONTACT WITH THE SEALANT
113
REFLOW THE SOLDER MATERIAL TO PHYSICALLY COUPLE THE LID TO THE DIE
115
CURE THE SEALANT
120
END

Fig. 4

SCHWEGMAN ■ LUNDBERG ■ WOESSNER ■ KLUTH

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **ELECTRONIC ASSEMBLY COMPRISING SOLDERABLE THERMAL INTERFACE AND METHODS OF MANUFACTURE**.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. § 1.56 (attached hereto). I also acknowledge my duty to disclose all information known to be material to patentability which became available between a filing date of a prior application and the national or PCT international filing date in the event this is a Continuation-In-Part application in accordance with 37 C.F.R. §1.63(e).

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 120 or 365(c) of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

No such claim for priority is being made at this time.

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Aldous, Alan K.	Reg. No. 31,905	Kalis, Janal M.	Reg. No. 37,650	Park, Ellen	Reg. No. 34,055
Anglin, J. Michael	Reg. No. 24,916	Kalson, Seth Z.	Reg. No. 40,670	Parker, J. Kevin	Reg. No. 33,024
Bianchi, Timothy E.	Reg. No. 39,610	Kaplan, David J	Reg. No. 41,105	Perdok, Monique M.	Reg. No. 42,989
Billion, Richard E.	Reg. No. 32,836	Kaufmann, John D.	Reg. No. 24,017	Prout, William F.	Reg. No. 33,995
Black, David W.	Reg. No. 42,331	Klima-Silberg, Catherine I.	Reg. No. 40,052	Reynolds, Thomas C.	Reg. No. 32,488
Brake, R. Edward	Reg. No. 37,784	Kluth, Daniel J.	Reg. No. 32,146	Schumm, Sherry W.	Reg. No. 39,422
Brennan, Leoniede M.	Reg. No. 35,832	Lacy, Rodney L.	Reg. No. 41,136	Schwegman, Micheal L.	Reg. No. 25,816
Brennan, Thomas F.	Reg. No. 35,075	Lam, Peter	Reg. No 44,855	Scott, John C.	Reg. No. 38,613
Brooks, Edward J., III	Reg. No. 40,925	Lemaire, Charles A.	Reg. No. 36,198	Seddon, Kenneth M.	Reg. No. 43,105
Burge, Ben	Reg. No. 42,372	LeMoine, Dana B.	Reg. No. 40,062	Seeley, Mark	Reg. No. 32,299
Chu, Dinh C.P.	Reg. No. 41,676	Lundberg, Steven W.	Reg. No. 30,568	Skabrat, Steven P.	Reg. No. 36,279
Clark, Barbara J.	Reg. No. 38,107	Maeyaert, Paul L.	Reg. No. 40,076	Skaist, Howard A.	Reg. No. 36,008
Clise, Timothy B.	Reg. No. 40,957	Maki, Peter C.	Reg. No. 42,832	Smith, Michael G.	Reg. No. 45,368
Dahl, John M.	Reg. No. 44,639	Malen, Peter L.	Reg. No. 44,894	Speier, Gary J.	Reg. No. 45,458
Draeger, Jeffrey S.	Reg. No. 41,000	Mates, Robert E.	Reg. No. 35,271	Steffey, Charles E.	Reg. No. 25,179
Drake, Eduardo E.	Reg. No. 40,594	McCrackin, Ann M.	Reg. No. 42,858	Su, Gene I.	Reg. No. 45,140
Embretson, Janet E.	Reg. No. 39,665	Mirho, Charles A.	Reg. No. 41,199	Terry, Kathleen R.	Reg. No. 31,884
Faatz, Cynthia Thomas	Reg. No. 39,973	Moore, Charles L., Jr.	Reg. No. 33,742	Tong, Viet V.	Reg. No. 45,416
Fordenbacher, Paul J.	Reg. No. 42,546	Nama, Kash	Reg. No. 44,255	Viksnins, Ann S.	Reg. No. 37,748
Forrest, Bradley A.	Reg. No. 30,837	Nelson, Albin J.	Reg. No. 28,650	Wells, Calvin E.	Reg. No. 43,256
Gamon, Owen J.	Reg. No. 36,143	Nielsen, Walter W.	Reg. No. 25,539	Werner, Raymond J.	Reg. No. 34,752
Greaves, John N.	Reg. No. 40,362	Novakoski, Leo V.	Reg. No. 37,198	Winkle, Robert G.	Reg. No. 37,474
Harris, Robert J.	Reg. No. 37,346	Oh, Allen J.	Reg. No. 42,047	Woessner, Warren D.	Reg. No. 30,440
Huebsch, Joseph C.	Reg. No. 42,673	Padys, Danny J.	Reg. No. 35,635	Young, Charles K.	Reg. No. 39,435
Jurkovich, Patti J.	Reg. No. 44,813				

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to **Schwegman, Lundberg, Woessner & Kluth, P.A.** at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402
Telephone No. (612)373-6900

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : **Biswajit Sur**
Citizenship: **India** Residence: **San Jose, CA**
Post Office Address: 6915 Rockton Avenue
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Signature: _____ Date: _____
Biswajit Sur

Full Name of joint inventor number 2 : **Nagesh Vodrahalli**
Citizenship: **United States of America** Residence: **Phoenix, AZ**
Post Office Address: 16207 South 13th Avenue
Phoenix, AZ 85045

Signature: _____ Date: _____
Nagesh Vodrahalli

X Additional inventors are being named on separately numbered sheets, attached hereto.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Post Office Address: 1430 Cherrydale Drive
San Jose, CA 95125

Signature: _____ Date: _____
Thomas Workman

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all informatio material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancel or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information know to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed b §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe an pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with th specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion o patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.